Tektronix[®]

Digital Pre-emphasis Processor

BERTScope® DPP Series Datasheet



BERTScope DPP125C Option ECM

Notice to EU customers

This product is not updated to comply with the RoHS 2 Directive 2011/65/ EU and will not be shipped to the EU. Customers may be able to purchase products from inventory that were placed on the EU market prior to July 22, 2017 until supplies are depleted. Tektronix is committed to helping you with your solution needs. Please contact your local sales representative for further assistance or to determine if alternative product(s) are available. Tektronix will continue service to the end of worldwide support life.

Features & Benefits

- 1 to 12.5 Gb/s for Support of Hardware-based Equalization of 2nd- and 3rd-generation Serial Standards
- 3- or 4-tap for Full Support of Compliance Testing for 802.3ap, Serial Attached SCSI, 10GBASE-KR Backplanes, DisplayPort[™], USB 3.0/3.1 PCI Express® Gen3
- Pre-cursor or Post-cursor Adjustment for Optimizing Compensation for ISI and Loss
- Exceptionally Easy Setup with Concurrent Multiple Domain Views Ideal for Operation as a Stand-alone Instrument Controlled by a Remote PC, or with a BERTScope for Complete Software Integration
- Precise Control to Correct for Effects such as Backplane ISI or Optical Effects with Adjustability through Tap Weights or Step Response provides the Flexibility Needed for Complete Design Characterization
- Optional integrated reference clock multiplication to PCIe compliant 2.5 GHz, 5 GHz, and 8 GHz
- Optional integrated eye opener functionality for testing DUTs with long
- Optional integrated clock doubler enables full rate stress for 12 Gb/s
- BERTScope Clock/Data delay compensated internally to allow lengthmatched cables
- Enclosure with the BERTScope footprint to allow equipment stacking

- New microcontroller to provide more processing power
- RS-232 interface enhancement to speed up PCIe receiver equalization link training

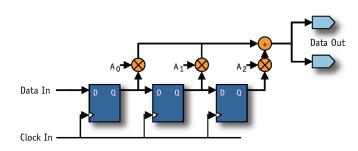
Applications

- Design Characterization for High-speed, Sophisticated Designs
- Certification Testing of Serial Data Streams for Industry Standards
- Design/Verification of High-speed I/O Components and Systems

Overview

The DPP125C is a nonlinear signal conditioner capable of adding controllable amounts of pre-emphasis to a signal. It takes in single-ended inputs of data and clock.





Example functional block diagram (3-Tap shown).

The BERTScope DPP Series can operate as a stand-alone instruments controlled by a PC, or with a BERTScope for complete software integration. It can be fully automated, and with its compact size, it will easily fit into a manufacturing environment.



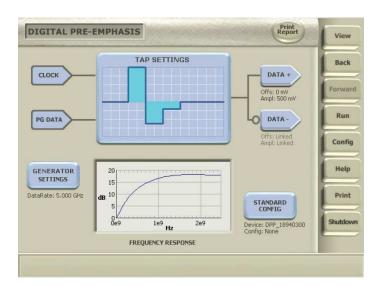
BERTScope DPP125C connected to a laptop

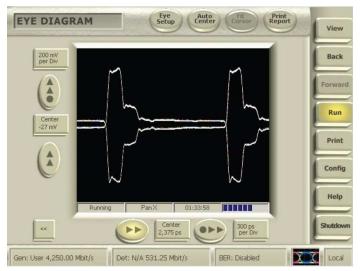


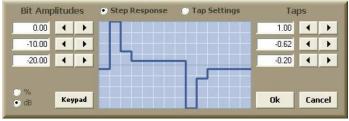
BERTScope DPP125C rear view

Intuitive control with many views

The wave shape can be adjusted in the user interface by either directly entering tap weights, or through an amplitude-weighted time domain bitmap showing the step response. In addition to these two views, a frequency-domain Bode plot is calculated and displayed to show the effect being implemented. This is particularly helpful when counteracting the effects of circuit board ISI with a measured frequency response.



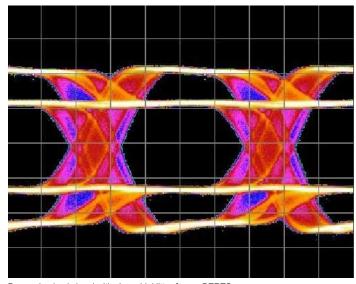




Intuitive user interface gives multiple views of the output waveform

Adjustable output

Output amplitude is user adjustable in amplitude and offset, and is offered differentially.



De-emphasized signal with sinusoidal jitter from a BERTScope

Specifications

All specifications are guaranteed unless noted otherwise. All specifications apply to all models unless noted otherwise.

Data rate range 1-12.5 Gb/s

Inputs

Clock Single-ended, SMA connector

250 mV Sensitivity (Typical)

 50Ω , AC coupled Termination

Maximum jitter transfer 1:1, Input clock to Output data

Data Single-ended, SMA connector

Sensitivity (Typical) 250 mV, PN31 pattern Termination 50Ω , AC coupled

Outputs

Data Differential, SMA connector

Maximum amplitude (Typical) 1.8 V, differential, adjustable

Differential skew (Typical) <2 ps ±500 mV Maximum DC offset (Typical)

Coupling AC, AC-coupled data with DC-coupled output offset

Function 3- or 4-tap, clocked FIR

<350 fs^{RMS}, additive, 1010 pattern Random jitter (Typical) -100 to +100 (including 0) in 1% steps Tap range

Tap resolution 1% or 0.1 dB, any tap **Transition time** <40 ps, all taps, 1010 pattern

Datasheet

General specifications

Control interface	USB 2.0	
Dimensions		
Width	39.4 cm (15.5 in)	
Height	9.5 cm (3.75 in)	
Depth	33.6 cm (13.25 in)	
Weight	4 kg (9 lb)	
Power consumption	<150 W	
Voltage	100-240 V AC, 45-63 Hz; Auto-range, IEC power plug	

Standards requirements

Standard	Required number of taps	Notes
802.3ap, 10GBASE-KR 10GbE Backplane	3	-
PCI Express 2.5 GT/s Receiver	2	0.7 dB for receiver testing
PCI Express 5 GT/s Transmitter	2	Selectable 3.5 dB and 6.0 dB levels on transmitters
PCI Express 8 GT/s	3	All preshoot and deemphasis settings in TxEQ coefficient matrix
SAS 6 Gb/s	2	2 dB for reference transmitters 2-4 dB for device transmitters
Display Port Transmitter 1.62 Gb/s and 2.7 Gb/s	2	Selectable 3.5 dB, 6 dB, or 9.5 dB on transmitters
USB 3.0 Transmitter 5 GT/s	2	3.5 dB nominal ±0.5 dB on transmitters

Ordering information

The BERTScope DPP Series can be operated stand-alone with a PC (not included) or with a suitable BERTScope model.

DPP125C

DPP125C 1-12.5 Gb/s 3-Tap Digital Pre-emphasis Processor

Instrument options

Opt. 4T Optional 4-Tap Digital Pre-emphasis Processor

Opt. ECM Optional integrated PCIe compliant clock multiplication for 2.5/5/8 GHz, eye opener, and clock doubler for 12 Gb/s SAS

Accessories

All models include: Power cable (US), USB cable, 2 SMA input cables, CD-ROM with software



Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.



Product Area Assessed: The planning, design/development and manufacture of electronic Test and Measurement instruments.

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